



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,301	05/30/2001	William J. Dally	81013 0269932	2038

7590 11/05/2004

ROBERT J. CRAWFORD
CRAWFORD MAUNU PLLC
1270 NORTHLAND DRIVE, SUITE 390
ST. PAUL, MN 55120

EXAMINER

MEONSKE, TONIA L

ART UNIT PAPER NUMBER

2183

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/871,301	Applicant(s) DALLY ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 18 and 19 is/are allowed.
- 6) ☒ Claim(s) 1-17 and 20-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9, 15-17, 22-24, and 26 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Asai et al., US Patent 5,553,309.

3. Claims 10-14, 20, 21, and 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Inagami et al., US Patent 4,881,168.

4. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action mailed on May 4, 2004.

Response to Arguments

5. Applicant's arguments filed August 9, 2004 have been fully considered but they are not persuasive.

6. On page 15, Applicant's argue in essence:

"With respect to independent claims 1, 7 8 9 15, and 17, the Office Action fails to provide a basis for alleging that the asserted '309 condition vector is a result "of evaluating a predetermined conditional expression," as claimed. The cited portions of the '309 figure 6 indicate the opposite of that which is asserted in the Office Action, i.e., the cited teachings indicate that the mask bits are independent. Applicant's review did not reveal how these mask bits are generated."

However, the condition vector, or mask register, of Asai et al. is in fact a result of evaluating a predetermined conditional expression. Applicant is directed to column 13, lines 56-64. The mask register is generated by evaluating a predetermined conditional

Art Unit: 2183

expression, whereby each component in the M register is compared to zero; Number “1” is stored in the mask register when the number is larger than zero and number “0” is stored in the mask register in all other cases. Therefore this argument is moot.

7. On page 16, Applicant’s argue in essence:

“With particular respect to claim 24, Applicant traverses the Section 102(b) rejection because the Office Action has not alleged any correspondence to, or presented any evidence as a basis for alleging that the ‘309 references teaches limitations relative to the claimed “plural clusters.” Without a showing of correspondence to each of the claimed limitations, the Section 102(b) rejection is improper and cannot be maintained.”

However, each element, or component, in an array is a processing cluster. For example, in Figure 6, component A(1) is a processing cluster that generates an output vector element A(1) in output vector register 2, component A(4) is a processing cluster that generates an output vector element A(4) in output vector register 2, and component A(5) is a processing cluster that generates an output vector element A(5) in output vector register 2, etc. Therefore this argument is moot.

8. On page 16, Applicant’s argue in essence:

“The Office Action alleges that the claimed buffer corresponds to item 3 of the ‘309 figure 1. However, item 3 of figure 1 is a general vector register which the flow diagram of figure 6 is intended to represent. Therefore, item 3 of figure 1 is not a separate register/buffer to which data is passed from the registers of figure 6.”

However, in claim 26, the limitation regarding the buffer reads “a buffer having a first plurality of entries and a second plurality of entries to store the input vector elements and the output vector elements.”. In this case, Asai et al. have taught a buffer having a first plurality of entries to store input vector elements, Figure 5, element 501, Figure 6, input vector register 1, and Asai et al. have taught a buffer having a second plurality of entries

Art Unit: 2183

to store output vector elements, Figure 5, elements 502 and 503, Figure 6, output vector register 3. Therefore this argument is moot.

9. On page 16, Applicant's argue with respect to claim 26 in essence:

"Moreover, the asserted vector device of figure 5 fails to correspond to the claimed controller because the figures fail to show a device that configures a switch "so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer.""

However, Claimed subject matter, not the specification, is the measure of invention.

Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978). In this case Applicant has not claimed *"a device that configures a switch "so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer" and as such this limitation is not read into the claims.* Therefore this argument is moot.

10. On page 16, Applicant's argue in essence:

"Applicant respectfully traverses the Section 102(b) rejection with respect to the '168 reference because the Office Action fails to present correspondence between each of the claimed limitations and the '168 reference. Regarding claims 10 and 11, the Office Action confusingly asserts that register 23 of Figure 4 is an input buffer with a length of 10 and also asserts that item 21 is the input vector having a length of 16."

However, the Office Action did not assert that register 23 of Figure 4 is an input buffer with a length of ten. Instead the Office Action stated that in Figure 4, element 21 is the input vector (page 16, section b.). For purposes of the office action, the input buffer consists of ten elements, A0-A9. Furthermore, the Office Action did not assert that item 21 is the input vector having a length of 16. In fact the Office Action instead asserted that the input vector has a length of 10 (page 16, section b.).

Art Unit: 2183

11. On page 16, Applicant's argue with respect to claims 10 and 14 in essence:

Claim 10 is directed to the length of the condition vector being greater than the length of the input vector. The '168 reference indicates that item 21 is the input vector having a length of 16. None of the remaining items of figure 4 identify a vector with a length of greater than 16, the asserted number of input vector elements.

However, the input buffer as defined by the Office Action consists of ten elements, A0-A9 in element 21. Thus the input buffer has a length of ten. The condition vector, element 22 contains sixteen elements. Therefore, Inagami et al. have taught that the length of the condition vector is greater than the length of the input vector. Therefore this argument is moot.

12. On page 16, Applicant's argue in essence:

Similarly regarding claims 12 and 13, these claims are directed to a number of clusters being greater than the number of input vector elements. None of the items of Figure 4 indicate a number of clusters greater than 16, the number of alleged input vector elements of item 21.

However, Inagami et al. have in fact taught a number of clusters being greater than the number of input vector elements. There are ten input vector elements, Figure 4, element 21 A0-A9. There are sixteen clusters, or sub-pipes, See column 6, line 37-column 7, line 13. The number of clusters is greater than the number of input vector elements.

Therefore this argument is moot.

13. On page 17, Applicant's argue in essence:

"Further regarding claims 20 and 21, the Office Action fails to identify where the '168 reference teaches "each arithmetic cluster completing processing of one input vector element before another input vector element is distributed to the arithmetic cluster." The cited portion of the '168 references teaches merely storing input vector data to alleged clusters and further fails to teach any iteration (claim 21)."

Art Unit: 2183

However, Inagami et al. have taught an iteration, see column 7, lines 8-14. In Inagami et al. the steps are repeated. Therefore this argument is moot.

Allowable Subject Matter

14. Claims 18 and 19 are allowed.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

16. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

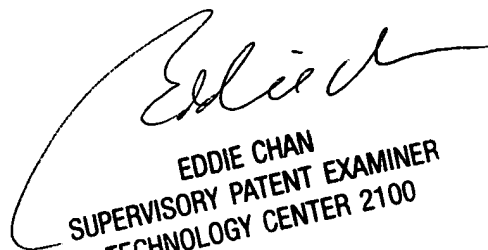
17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2183

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100